

13 floating gate [therefrom] by [a] said second insulation layer, at least a portion of said control gate
14 being disposed over a portion of said substrate and being separated therefrom by said second
15 insulating layer;

16 an erase gate [generally placed on a second side] formed over a second one of said side
17 walls and over at least a portion of said top surface of said floating gate and being separated
18 [therefrom] from said second one of said side walls by said second insulation layer;

19 a drain region formed in a portion of said substrate proximate said control gate [generally
20 disposed on a first side of said floating gate]; and

21 a source region [generally disposed on a second side of said floating gate] formed in a
22 portion of said substrate proximate said erase gate.

1 8. (Once Amended) A memory array disposed on a substrate comprising a plurality of memory
2 cells each having a floating gate separated from said substrate by a first insulating layer, an erase
3 gate, a control gate separated from said floating gate by a second insulating layer, a source
4 region, and a drain region, comprising:

5 a plurality of rows and columns of interconnected memory cells wherein the control gates
6 of memory cells in the same row are connected by a common word-line, the erase gates of the
7 memory cells in the same rows are connected by a common erase line, [and] the source regions
8 of the memory cells in the same rows are connected by a common source line, and the drain
9 regions of memory cells in the same columns are commonly connected via a common drain line,
10 wherein at least a portion of each said control gate is disposed over a portion of said substrate
11 and separated therefrom by said second insulating layer; and

12 control circuit connecting to said word-lines, erase lines, source lines and drain lines for
13 operating one or more memory cells of said memory array.

1 16. (New) A semiconductor device having at least one transistor, the device comprising:
2 a substrate having a channel region;
3 a first insulating layer disposed over said channel region and over at least a portion of
4 said substrate;

5 a floating gate generally disposed over said channel region and separated therefrom by
6 said first insulating layer, said floating gate having at least two side walls and a top surface;